## REMARKS

Generic claims 1-4 and species claim 8 are pending before the Examiner. Species claims 5-7 are subject to a restriction requirement and are withdrawn without prejudice.

Claim 1 is amended and claim 2 is cancelled. Support for the amendment is found in the specification and the claims as originally filed. No new matter is added.

Claims 1-8 are rejected under 35 U.S.C. §103 (a) as being unpatentable over either Chen et al. (5,858,869) or Lou (5,759,906). Applicants traverse the rejection to the extent that it can be maintained. Claim 2 is cancelled. Claims 5-7 are withdrawn.

Briefly, Applicant's invention is a method for forming a multi-layer wiring structure, for example for a semiconductor device, using the "damascene process". In the damascene process the interconnect pattern for metal conductors is first lithographically defined in an insulating layer of dielectric, the lithographic resist mask is removed by an ashing process and metal is deposited to fill the resulting trenches. Excess metal is removed by means of chemical-mechanical polishing (planarization). Additional layers may be built by repeating these steps. Ultra Large Scale Integration requires the spacing between metal on the same layer and between metal on adjacent layers to be minimized. As the spacing between metal lines decreases, the capacitance between metal lines increases and adversely affects the performance of the circuit. By forming insulating layers from material having a low dielectric constant, such as organic or inorganic SOG, the capacitance can be reduced to offset the adverse effect from more closely spaced metal lines. However, the ashing process using an oxygen plasma to remove the resist mask may affect the chemical structure of the insulating layer thereby increasing the dielectric constant. Applicant discovered that the low dielectric constant of the insulating layer can be maintained by removing the resist used in the damascene method by an ashing process using oxygen plasma under an atmospheric pressure from 0.01 to 30 Torr.

As a preliminary matter, neither Chen et al. nor Lou form a multi-layer wiring structure using the damascene method. Both Chen et al. and Lou form a wiring pattern on a pad $SiO_2$ layer and then add insulating layers to the wiring pattern. Vias are formed for wiring connections between layers. Both Chen et al. and Lou recognize the need for insulating layers

with a low dielectric constant in highly integrated circuits. However, each achieves low dielectric constant interlayer dielectrics (ILDs) by different means and means different from that claimed by Applicant. Specifically, Lou forms a wiring pattern on a first insulating layer on a semiconductor substrate and then forms a multi-layer ILD composed of at least four low dielectric constant polymer layers on the wiring pattern (e.g. column 4 lines 6-24). Lou does not disclose conditions for removing resist nor does Lou recognize the adverse effect on the ILD if the resist is removed by ashing using an oxygen plasma. Chen et al. form a wiring pattern on a first insulating layer on a semiconductor substrate and then deposit an anisotropic plasma oxide layer on the wiring pattern. A low dielectric constant insulator is deposited on the anisotropic plasma oxide layer. The low dielectric constant insulator is polished back and a fluorine-doped oxide is deposited on the insulator (e.g. column 5 line 62 to column 5 line 54). The anisotropic plasma oxide layer enables wider openings between conductors in the wiring pattern thereby allowing a greater amount of low dielectric polymer to be deposited between conductors (e.g. column 7 line 32 to column 8 line 9). Like Lou, Chen et al. do not disclose conditions for removing resist nor do Chen et al. recognize the adverse effect on the ILD if the resist is removed by ashing using an oxygen plasma. The cited references do not teach or suggest Applicant's invention as a whole. Examiner asserts that the damascene process is simply an alternative method for forming an ILD layer and within the knowledge of one skilled in the art. However, in the damascene process the wiring pattern is etched into the ILD layer rather than forming the ILD layer on the wiring as taught by Chen et al. and Lou. Ashing the resist using prior art methods of Chen et al. and Lou does not expose the ILD layer to the ashing plasma. Examiner has not explained the reason the skilled artisan with no knowledge of the claimed invention would have been motivated to perform the ashing process to remove the resist from the ILD layer using oxygen gas plasma under an atmospheric pressure from 0.01 Torr to 30.0 Torr to avoid an adverse effect on the low dielectric constant of the ILD layer. Applicant respectfully asserts that neither Lou nor Chen et al. combined with the knowledge of a skilled artisan teaches or suggests applicant's invention as a whole, and requests that the rejection on this ground be withdrawn.

Applicants respectfully submit that the present application is in condition for allowance, and prompt passage to issue is earnestly solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned VERSION WITH MARKINGS TO SHOW CHANGES MADE.

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

### In the Claims

1. (AMENDED) A method for forming a multi-layer wiring structure, comprising the following steps:

(a) etching to form via-holes or wiring gutters through a resist mask on an insulating film between layers of a silica system having a dielectric constant being equal to or less than 3.5;

(b) filling up said wiring gutters or said via-holes with conductive material using a damascene method; and

(c) performing an ashing process on said resist mask using oxygen gas plasma under an atmospheric pressure from 0.01 Torr to 30.0 Torr.

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